



PATENT

IFW

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Ligang Zhang, et al.

Title: REDISTRIBUTION LAYER SHIELDING OF A CIRCUIT ELEMENT

Application No.: 10/814,816

Filed:

March 31, 2004

Examiner: Jennifer E. Matisiak

Group Art Unit:

2811

Atty. Docket No.: 026-0041

Confirmation No.:

5295

September 23, 2005

Mail Stop Amendment  
COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, VA 22313-1450

**INFORMATION DISCLOSURE STATEMENT****37 C.F.R. § 1.97(b)**

Dear Sir:

Pursuant to 37 C.F.R. § 1.56, § 1.97 and § 1.98, the undersigned brings to the Examiner's attention in the above-identified application the patents, publications, applications or other information identified in the attached:

- ☒ Form(s) PTO/SB/08A (1 page(s), with copy of no reference(s)).
- ☒ Form(s) PTO/SB/08B (1 page(s), with copy of 10 reference(s)).
- ☐ Listing of Pending Applications (N/A page(s), with copy of no application(s)).
- ☐ Other: N/A

Citation of such information shall not be construed as (i) an admission that the information necessarily is, or corresponds to, prior art with respect to the instant invention, (ii) a representation that a search has been made, other than as described herein, or (iii) an admission that the information cited herein is, or is considered to be, material to patentability as defined in § 1.56(b).

For each item of information listed that is not in the English language, the undersigned has provided a concise explanation of the relevance through (i) an English language abstract, (ii) an English language equivalent application, or (iii) if cited in a search report or other action by a foreign patent office in a counterpart foreign application, an English language version of the search report or action that indicates the degree of relevance found by the foreign office.

CERTAIN COPIES NOT INCLUDED

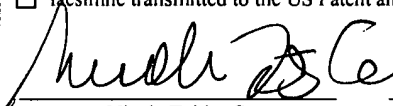
Pursuant to operative regulations, certain copies need not be provided and corresponding information is identified in this Information Disclosure Statement by citation only. In particular,

- ☒ In accordance with 37 C.F.R. § 1.98(a)(2)(ii), copies of cited U.S. Patents and U.S. Patent Application Publications are not included.
- ☐ Certain information was submitted to, or cited by, the Office in Application No(s). N/A, filed N/A, to which the above-identified application claims priority under 35 U.S.C. § 120. In accordance with 37 C.F.R. § 1.98(d), copies of that information are not included.
- ☐ Pursuant to 1287 OG 163 (October 19, 2004), for those cited pending U.S. patent applications filed (or which entered the national stage under 35 U.S.C. § 371) on or after June 30, 2003 or which are otherwise stored in the USPTO's Image File Wrapper system, copies are not included.

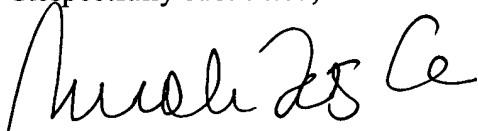
FEE AUTHORIZATION

- ☐ This Information Disclosure Statement is filed within three months of the filing date of a national application other than a continued prosecution application under § 1.53(d) or within three months of entry of the national stage as set forth in § 1.491 in an international application. Therefore, no fee is required.
- ☒ The undersigned believes that this Information Disclosure Statement is being filed before the mailing date of a first Office action on the merits or before the mailing date of a first Office action after the filing of a request for continued examination under § 1.114. Therefore, no fee is believed required.

If however, this Information Disclosure Statement is filed after the period specified in § 1.97(b), the undersigned hereby authorizes the Commissioner to charge the fee set forth in § 1.17(p) to Deposit Account No. 50-0631.

<u>CERTIFICATE OF MAILING OR TRANSMISSION</u>	
I hereby certify that, on the date shown below, this correspondence is being	
<input checked="" type="checkbox"/>	deposited with the US Postal Service with sufficient postage as first class mail and addressed as shown above.
<input type="checkbox"/>	facsimile transmitted to the US Patent and Trademark Office.
	<u>9/23/05</u>
Nicole Teitler Cave	Date

Respectfully submitted,

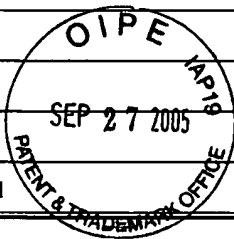


Nicole Teitler Cave, Reg. No. 54,021  
 Attorney for Applicant(s)  
 (512) 338-6315 (direct)  
 (512) 338-6300 (main)  
 (512) 338-6301 (fax)

EXPRESS MAIL LABEL: \_\_\_\_\_



PTO/SB/08B (Substitute for form 1449/PTO)		Attorney Docket No.: 026-0041
		Application No.: 10/814,816
INFORMATION DISCLOSURE STATEMENT BY APPLICANT		First Named Inventor: Ligang Zhang
		Filing Date: March 31, 2004
		Group Art Unit: 2811
		Examiner Name: Jennifer E. Matisiak
Sheet 1 of 1		Date Submitted: September 23, 2005



### NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. <sup>1</sup>	Include name of author (in CAPITAL LETTERS), title of article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
	AA	FROMMBERGER, Michael, et al., "Integration of Crossed Anisotropy Magnetic Core Into Toroidal Thin-Film Inductors," IEEE Transactions on Microwave Theory and Techniques, Vol. 53, No. 6, June 2005, pp. 2096-2100.	
	AB	KIM, Sung-Jin, et al., "Realization of High-Q Inductors Using Wirebonding Technology," School of Electronics Engineering, Ajou University, AP-ASIG Proceedings, August 1999, 4 pages.	
	AC	LONG, John R. and Miles A. Copeland, "The Modeling, Characterization, and Design of Monolithic Inductors for Silicon RF IC's," IEEE Journal of Solid-State Circuits, Vol. 32, No. 3, March 1997, pp. 357-369.	
	AD	SOH, H. T., et al., "Through-Wafer Vias (TWV) and their Applications in 3 Dimensional Structures," Proceedings of 1998 International Conference on Solid State Devices and Materials, September 1998, 12 pages.	
	AE	TANG, Chih-Chun, et al., "Miniature 3-D Inductors in Standard CMOS Process," IEEE Journal of Solid-State Circuits, Vol. 37, No. 4, April 2002, pp. 471-480.	
	AF	TRELEAVEN, Dave and Dick James, "Integrated Circuit Passive Components," Whitepapers, Chipworks, <a href="http://www.chipworks.com/resources/resources_whitepapers.asp">www.chipworks.com/resources/resources_whitepapers.asp</a> , 4 pages.	
	AG	TSUI, Hau-Yiu and Jack Lau, 2003 IEEE MTT-S Digest, pp. 225-228.	
	AH	WU, Joyce H., et al., "A Through-Wafer Interconnect in Silicon for RFICs," IEEE Transactions on Electron Devices, Vol. 51, No. 11, November 2004, pp. 1765-1771.	
	AI	ZANNOTH, Markus, et al., "A Fully Integrated VCO at 2 GHz," IEEE Journal of Solid-State Circuits, Vol. 33, No. 12, December 1998, pp. 1987-1991.	
	AJ	ZOU, Jun, et al., "Development of Vertical Planar Coil Inductors Using Plastic Deformation Magnetic Assembly (PDMA), 2001 IEEE International Microwave Symposium, May 2001, 4 pages.	
Examiner Signature		Date Considered	

\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

<sup>1</sup>Applicant's unique citation designation number (optional).

<sup>2</sup>Applicant is to place a check mark here if English language Translation is attached.